IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC. *Plaintiff,*	§	
vs.	§	Civil Action No. 4:03-CV-276
MOTOROLA, INC. *Defendant, Counterclaim Plaintiff*	§	Judge Leonard E. Davis
vs.	§	
STMICROELECTRONICS, N.V., AND STMICROELECTRONICS, INC. *Counterclaim Defendants*	§	Jury Trial Demanded

STMICROELECTRONICS, N.V. AND STMICROELECTRONICS, INC.'S MOTION TO ENFORCE MOTOROLA INC.'S COMPLIANCE WITH PATENT RULE 3-1, AND BRIEF IN SUPPORT THEREOF

STMicroelectronics, NV ("ST NV") and STMicroelectronics, Inc. ("ST INC") move to enforce Motorola Inc.'s ("Motorola") compliance with patent rule 3-1 ("P.R. 3-1") in accordance with this Court's October 30, 2003, Docket Control Order ("Docket Order"). P.R. 3-1 requires Motorola to disclose the bases for its contentions that ST NV and ST INC allegedly infringed Motorola's patents-in-suit ("Infringement Contentions" or "Contentions"). Motorola's Infringement Contentions pertaining to two of its four patents-in-suit, U.S. Patent No. 5,084,814 (the " '814 patent") and U.S. Patent No. 4,548,654 (the " '654 patent"), fail to comply with P.R. 3-1 because they (1) do not show how each of the elements of Motorola's claims compare to specific ST NV or ST INC products and (2) do not identify specifically by name either the allegedly infringing processes or the products made by these processes.

ST NV and ST INC brought these deficiencies to Motorola's attention and requested supplementation or amendment of Motorola's Contentions. Motorola has not supplemented its contentions, necessitating the filing of this motion. In failing to provide the disclosures required by P.R. 3-1, Motorola severely prejudices ST NV and ST INC in their ability to assess Motorola's claims and pursue meaningful discovery in a case with expert report deadlines in June and July and a trial set for November of 2004. Therefore, ST NV and ST INC reluctantly seek this Court's intervention.

I. Relevant Factual Background

ST INC brought this action against Motorola on July 18, 2003, claiming infringement of three of its patents. On September 11, 2003, Motorola responded by counterclaiming for infringement of four of its patents by ST INC and ST INC's parent corporation, ST NV.[1]

This Court's Docket Order required Motorola to file its Infringement Contentions by October 31, 2003. Though Motorola filed its Contentions, it failed in significant part to comply with P.R. 3-1. ST NV advised Motorola of the deficiencies in its Contentions. *See* January 12, 2004, Letter from J. Bradley to H. Galvan attached hereto as Exhibit 1 and incorporated by reference. ST NV conferred with Motorola's counsel about the concerns outlined in its January 12, 2004 letter regarding the supplementation or amendment of Motorola's Contentions by telephone on January 16, 2004, by email on January 20, 2004, and again by letters on January 21 and January 30, 2004. *See* January 21, 2004 and January 30, 2004, Letters from J. Bradley to H. Galvan attached hereto as Exhibit 2 and incorporated by reference. As a result of such

[1] Motorola improperly counterclaimed against ST NV rather than properly asserting infringement claims against ST NV. Rather than contest Motorola's "counterclaims" and waste valuable Court resources with a motion to dismiss for improper joinder, ST NV accepted service

conferences, Motorola admitted that it did not possess information sufficient to determine whether ST NV or ST INC infringe the claims of Motorola's '654 Patent. *See* January 22, 2004, Letter from H. Galvan to J. Bradley attached hereto as Exhibit 3 and incorporated by reference. Motorola initially declined to supplement or amend its Contentions, insisting that it had complied fully with the requirements of P.R. 3-1, and it has since offered to supplement its contentions by February 16, 2004. *See* January 28, 2004, Letter from H. Galvan to J. Bradley attached hereto as Exhibit 4 and incorporated by reference.

This matter is set for trial on November 1, 2004. ST INC and Motorola collectively assert infringement of seven patents. In order to proceed in this litigation, ST NV and ST INC need to know what products or processes are at issue and how each element of the asserted claims are found in these allegedly infringing products or processes. These are the most basic disclosures required by P.R. 3-1.

II. Argument

The rules of practice for patent cases apply to all actions filed in this Court which allege infringement of a utility patent. P.R. 3-1 sets forth the requirements for disclosing preliminary infringement contentions; this rule takes the place of "a series of interrogatories that [an alleged infringer] would likely have propounded had the patent local rules not provided for streamlined discovery." *Network Caching Tech., LLC v. Novell, Inc.*, No. C-01-2079-VRW, 2002 U.S. Dist. LEXIS 26098, at *12 (N.D. Cal. August 13, 2002).

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and entered this action as a "counterclaim defendant."

Motorola contends that ST INC and ST NV infringed its '814 and '654 Patents. P.R. 3-1 identifies the following categories of information that must be contained in Motorola's Preliminary Contentions:

> (a) Each claim of each patent in suit that is allegedly infringed by each opposing party,
>
> (b) Separately for each asserted claim, each accused apparatus, product, device, process, method, act, or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. This identification shall be as specific as possible. Each product, device, and apparatus must be identified by name or model number, if known. **Each method or process must be identified by name, if known, or by any product, device, or apparatus which, when used, allegedly results in the practice of the claimed method or process**, [and]
>
> (c) A chart identifying specifically **where each element of each asserted claim is found within each Accused Instrumentality** . . . .

P.R. 3-1(a)-(c) (emphases added).

Motorola's Infringement Contentions for the '814 and '654 patents fail to comply with (1) P.R. 3-1(c) by not showing where each element of Motorola's claims is found within each ST NV or ST INC product and (2) P.R. 3-1(b) by not identifying by name allegedly infringing processes, or products of processes.

A. Contrary to P.R. 3-1(c), Motorola does not show where each element of its patent claims is found within each ST NV or ST INC product or process

P.R. 3-1(c) requires a party asserting patent infringement to chart out where each element of its patent claims is found within each allegedly infringing product or process. This requires that the party "compare an accused product to its patents on a claim by claim, element by element basis for at least one of [] [the alleged infringer's] products." *Network Caching Tech., LLC*, 2002 U.S. Dist. LEXIS 26098 at *16. "To the extent [a party asserting infringement], for whatever reason, do[es] not yet know where an element of a claim is found within a particular

product, they should so state in their initial [P.R. 3-1] disclosure." *Hewlett-Packard Co. v. EMC Corp.*, No. C 02-04709 JF (PVT), 2003 U.S. Dist. LEXIS 22742, at *4 (N.D. Cal. July 9, 2003).

A reasonable inquiry must be made into the applicable facts and law before filing P.R. 3-1 disclosures. *Network Caching Tech., LLC*, 2002 U.S. Dist. LEXIS 26098 at *12-*16. Such reasonable inquiry requires that the party asserting infringement reverse engineer the accused products or perform an equivalent, detailed analysis of the products. *See id.* at *16; *Intertrust Tech. Corp. v. Microsoft Corp.*, No. C 01-1640 SBA, 2003 U.S. Dist. LEXIS 22736, at *7 (N.D. Cal. Nov. 26, 2003).

In *Network Caching*, the plaintiff based its infringement claims on the defendant's white paper and marketing materials. 2002 U.S. Dist. LEXIS 26098. The plaintiff did not reverse engineer the defendant's software. The court found that the level of detail provided in the plaintiff's P.R. 3-1(c) charts was "plainly insufficient":

> [Plaintiff] provides no link between the quoted passages [of the marketing literature] and the infringement contention that simply mimics the language of the claim. The courts see no specific link. For example, [plaintiff] provides no explanation of how the proxies described in the literature map onto the claim language. Nor does [plaintiff] describe how 'couple cluster technology' is relevant. In essence, [plaintiff] has provided no further information to defendants than the claim language itself. This is plainly insufficient.

Id. at *18.

The charts attached to Motorola's '814 Patent and '654 Patent Infringement Contentions fail to reference any specific products or processes of ST NV or ST INC. *See* Exhibits B and C of Motorola's Disclosure of Asserted Claims and Preliminary Infringement Contentions, attached hereto as Exhibit 5 and incorporated by reference. In the left hand column of its charts, Motorola sets out the language of the elements of its patent claims. Then in the right hand

column, Motorola largely repeats its claim element language verbatim in reference to broad categories of "STMicro" or "STM"[2] products, or, in the case of the '654 patent,[3] no category of products. *See id.*

Motorola's '814 and '654 Patent Contention charts do not comply with the level of specificity required by P.R. 3-1(c). For example, Motorola claims that "STMicro" products containing ARM 7, ARM 9, ARM 10, and ARM 11 processor family cores infringe the claims of its '814 Patent. *See id.* Setting aside the impropriety of Motorola's broad ARM family core product designations, Motorola's '814 Patent chart only compares ARM 7 family core products to the elements of its patent claims. Footnote 1 of Motorola's '814 chart states that analyses for ARM 9, 10, and 11 family cores are similar. *See* Exhibit 5 at fn. 1. Such sweeping allegations do not comply with the specificity requirements of P.R. 3-1(c). *See Intertrust Tech.*, 2003 U.S. Dist. LEXIS 22736 at *7; *Network Caching Tech.*, 2002 U.S. Dist. LEXIS 26098 at *16.

Further, Motorola's broad "STMicro" product references are "supported" by citations to entire chapters and figures of technical documents from ARM Limited, the developer of the ARM 7 processors. *See* Exhibit 5. For example, at row 1C of the chart for the '814 Patent, Motorola contends that the ARM 7 processor "includes serial debug pins that are used only for development support functions." *See id.* Motorola then attempts to bolster this general allegation with references to four chapters and several figures in an ARM data sheet and an ARM technical reference manual. *See id.* However, Motorola does not identify the "serial debug pins that are used only for development support functions" that Motorola apparently

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[2] Motorola's "STMicro" and "STM" designations reference a collective entity consisting of ST INC and ST NV.

[3] The '654 Patent chart does not reference by name any ST NV or ST INC process or any third-

claims exist in the ARM7 core processor. Motorola must "identify specifically where each element . . . is found within each Accused Instrumentality" to comply with the patent rules. Motorola cannot just incorporate whole chapters of ARM manuals, thereby placing the burden on ST NV and ST INC to discern the specific location of the claim element within the ARM7 processors.

The above is only one example. Motorola's '814 and '654 Patent Contentions are general allegations purportedly supported by mere references to chapters and figures of broad product manuals. Currently, Motorola's '814 and '654 Contention charts provide no further information to ST NV and ST INC than the claim language itself and hinder ST NV and ST INC in their ability to assess Motorola's claims and pursue meaningful discovery. Therefore, ST NV and ST INC request that this Court enforce P.R. 3-1(c) and require Motorola supplement its '814 and '654 Patent Contention charts and properly set forth information on ST NV or ST INC's products or processes. Specifically, Motorola should set forth where each element of Motorola's asserted '814 and '654 Patent claims is found within each accused ST NV or ST INC product or process.

B. Contrary to P.R. 3-1(b), Motorola does not identify by name allegedly infringing processes, or products of processes

P.R. 3-1(b) requires a party claiming infringement to identify each allegedly infringing process or product. This identification should be as specific as possible, and each process must be identified by name, if known, or by any product resulting from the process. *See* P.R. 3-1(b).

In its '654 Patent Contentions, Motorola contends the STMicro products or processes that violate claims 1-7 and 9 of its '654 patent are "processes used by or for STM which include the

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party wafer suppliers' process.

step of heating a silicon wafer or substrate in a reducing ambient and a later step of heating the wafer or substrate at a lower temperature, and the STM products that are made thereby." *See* Exhibit 5 (emphasis added). This generic identification does not alert ST NV or ST INC as to the bases for Motorola's claim of infringement.

A quick review of the claim chart for the '654 Patent shows that it is devoid of meaningful information as to the bases for Motorola's contention of infringement. The chart only references "the accused processes," but it never identifies the process or processes. Motorola fails to say whether the alleged processes are carried out by "STMicro" or whether these processes are carried out in the wafer foundry of a third party. Apparently, Motorola does not know whether ST NV or ST INC products or processes infringe the claims of its '654 Patent. *See* Exhibit 3.

Motorola's reasonable inquiry prior to filing its '654 Patent Contentions should have uncovered, at the least, the identity of ST NV or ST INC processes or products that allegedly infringe Motorola's '654 Patent. *See Intertrust Tech.*, 2003 U.S. Dist. LEXIS 22736 at *7 (A party claiming infringement must "make a reasonable inquiry into the applicable facts and law before filing a document, such as Patent Local Rule 3-1 Disclosures."). Without the identity of an accused process or product, ST NV and ST INC cannot formulate their defenses and engage in meaningful discovery pertaining to the '654 Patent. ST NV and ST INC cannot produce documents or answer interrogatories concerning such unidentified processes and products, nor can they prepare expert reports. Thus, ST NV and ST INC will suffer severe prejudice if Motorola does not supplement its '654 Patent Contention and identify specifically processes, or products of processes, that allegedly infringe the '654 Patent.

III. Conclusion

ST NV and ST INC regret seeking Court intervention on these matters. Due to the accelerated schedule in this action and the substantial deficiencies in Motorola's Infringement Contentions, ST NV and ST INC are forced to file this motion seeking enforcement of P.R. 3-1. Therefore, in accordance with this motion, ST NV and ST INC request that Motorola supplement its Infringement Contentions with respect to the '814 and '654 Patents and (1) set forth where each element of Motorola's asserted '814 and '654 Patent claims is found within each allegedly infringing ST NV or ST INC product, and (2) identify specifically processes, or products of processes, that allegedly infringe Motorola's '654 Patent.

Respectfully submitted,

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ATTORNEYS FOR PLAINTIFF AND COUNTERCLAIM DEFENDANT STMICROELECTRONICS, INC.

CERTIFICATE OF CONFERENCE

Counsel for STMicroelectronics, NV and ST Microelectronics, Inc. have conferred with the undersigned counsel for Motorola, Inc. in a good faith attempt to resolve this matter without Court intervention. Counsel for STMicroelectronics, NV made additional efforts to contact counsel for Motorola, Inc. on January 22 and 23, by telephone and email to discuss the matter further, but STMicroelectronics, NV has not received a response as of this time. The parties have been unable to resolve the issues raised in STMicroelectronics, NV and STMicroelectronics, Inc.'s motion to enforce Motorola Inc.'s compliance with patent rule 3-1; therefore, this motion is opposed.

JAMES P. BRADLEY

CERTIFICATE OF SERVICE

I certify that a copy of the foregoing *STMicroelectronics, N.V. and STMicroelectronics, Inc.'s Motion to Enforce Motorola's to Enforce Motorola Inc.'s Compliance with Patent Rule 3-1, and Brief in Support Thereof* was served this 30th day of January 2004 upon the following counsel of record, as follows:

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January 12, 2004

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VIA FACSIMILE

Re: *STMicroelectronics, Inc. v. Motorola, Inc. v. STMicroelectronics N.V. and STMicroelectronics, Inc.* Civil Action No. 4:03-CV-276 (Sherman)

Dear Hilda:

Motorola's Disclosure of Asserted Claims and Preliminary Infringements Contentions fails to comply with the disclosures required by Local Rule P.R. 3-1(a)-(d) and (f) for the reasons noted below. In view of the accelerated schedule for this matter, we ask that Motorola promptly amend or supplement its preliminary infringement contentions. If Motorola declines to do so, please advise us of that fact now so we can, if necessary, bring this deficiency to the Court's attention.

Local Rule P.R. 3.1(a)-(c) requires Motorola to identify each claim that is allegedly infringed by each opposing party. However, Motorola's preliminary infringement contentions do not attempt to identify STNV products or processes, rather Motorola ignores the rules and lists products it attributes to both defendants.

Motorola also fails to comply with Local Rule P.R. 3-1(d), which requires Motorola to state whether each element of "each asserted claim is claimed to be literally present or present under the doctrine of equivalents in the Accused Instrumentality." Motorola's assertion that both defendants infringe "the asserted claims literally and/or by the Doctrine of Equivalents" is meaningless and does not provide the necessary details of a patentee's infringement contentions called for by this rule. Motorola must now identify in its preliminary infringement contentions whether the alleged infringement is literal or under the doctrine of its equivalents, and Motorola must do this for "each element of each asserted claim." (emphasis added) Further, Motorola must apply this rule with respect to the Accused Instrumentality for each defendant.

In addition to the above, Motorola fails to comply with Local P.R. 3-1 in its other assertions involving the '814 patent. Motorola's footnote reference in its infringement claim chart that the analysis of the ARM 9 Family is "similar" does not comply with the rule. Further, Motorola's statement that upon "information and belief" the analysis for products containing the ARM 10 and 11 Family is similar to the ARM 7 is insufficient information, and it does not bring the ARM 9, ARM 10 and ARM 11 Family cases into issue in this case.

In addition to the above, Motorola's contentions are also deficient in failing to follow Local Rule P.R. 3-1 with respect to the'694 patent. Motorola's allegations that "Processes used by or for STM" is vague and insufficient. P.R. 3-1(b) requires that each accused process "must be identified by name, if known, or by product, device or apparatus, which, when used allegedly results in the practice of the claimed method or process." Motorola does not identify by name any process allegedly used by a third party supplying wafers to STNV. Motorola's claim charts also fail to identify any process of STNV by name or any product allegedly made by STNV allegedly using any claimed process.

In view of the tight schedule which we are all working under, we will call you later today or tomorrow to discuss whether Motorola will agree to immediately provide its preliminary infringement contentions and comply with the Patent Rules. We look forward to receiving your cooperation in this matter.

Very truly yours,

James P. Bradley

JPB/bls

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January 21, 2004

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Re: *STMicroelectronics, Inc. v. Motorola, Inc. v. STMicroelectronics N.V. and STMicroelectronics, Inc.* Civil Action No. 4:03-CV-276 (Sherman)

Dear Hilda:

We are writing to follow up on our prior correspondence and telephone call regarding our request that Motorola provide additional facts in its infringement contentions in order to comply with Local Patent Rule 3-1.

We understood from our call on Friday that you would be providing us at least the identity of the wafers which Motorola accuses to be an infringement of the Tobin '654 patent. However, you sent us an e-mail yesterday stating, "On the Tobin issue, I did not state that we would identify the accused wafers." We ask that you reconsider your position and promptly identify accused wafers, any accused process practiced by the wafer manufacturers, or any accused process(es) practiced by either of the defendants.

Also, we renew our request that you reconsider providing ST NV with more specific information in the claim charts for the Vaglica '814 patent. As an example, in element C of Claim 1, Motorola does not identify by pin name the "plurality of pins" in its reference to materials for the ARM 7 RISC processor. In addition, Motorola has not provided any infringement claim charts for the ARM 9, ARM 10, or ARM 11 cores.

If Motorola continues to refuse to provide preliminary infringement contentions required by P.R. 3-1, ST NV will be forced to approach the Court for relief.

We appreciate your further consideration of this matter.

Yours truly,

James P. Bradley

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January 30, 2004

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Re: *STMicroelectronics, Inc. v. Motorola, Inc. v. STMicroelectronics N.V. and STMicroelectronics, Inc.* Civil Action No. 4:03-CV-276 (Sherman)

Dear Hilda:

I called you last Friday, January 23, 2004, in an another effort to have Motorola comply with Patent Rule 3-1. When I did not receive supplemental infringement contentions for Tobin on Tuesday, the date I understood you would provide these, I decided to send you an e-mail that set forth our understanding of your offer to supplement Motorola's infringement contentions and claim charts for the Tobin and Vaglica patents. We were surprised to receive your letter Wednesday evening with your different understanding of what Motorola agreed to do. Leaving the differences aside on our understanding from the call, we continue to seek Motorola's infringement contentions that are required by P.R. 3-1.

The Tobin '654 Patent

With respect to the Tobin '654 patent, you stated on our call that you were unable to identify at this time any ST Inc. or ST NV process that infringes the '654 patent. You were also unable to identify any wafer purchased by ST Inc. or ST NV that was used in fabricating a semiconductor device that you contend infringes the '654 patent. We understood you to say that you agreed to identify the wafers purchased by ST Inc. or ST NV that you contend infringe the Tobin '654 patent by last Tuesday. The offer you make in Wednesday's letter for Motorola to provide information regarding wafers used in Motorola products that practice the claimed invention is entirely different and not in compliance with the rules. P.R. 3-1(f) gives a patentee the option of identifying its own products that practice its patents, but this does not put Motorola in compliance with P.R. 3-1(c).

In view of the fact that Motorola has failed to identify any product or process that infringes the '654 patent, it is clear that Motorola has failed to comply with P.R. 3-1(b) or P.R. 3-1(c). We feel we have now exhausted our efforts to have Motorola fulfill its obligations under P.R. 3-1, and, thus, you leave us with no choice but to seek the Court's assistance in this matter.

The Vaglica '814 Patent

On January 23, we also met and conferred regarding Motorola's deficiencies in its infringement contentions for the '814 patent. In addition to failing to include any ST Inc. or ST NV products in the charts, the charts were deficient in failing to identify where each element was found in the ARM 7 cores. We understood you agreed to provide infringement claim charts for the Vaglica '814 patent as you apply it to ST Inc. or ST NV products by Friday, January 30, 2004. You now inform us that you will not provide these infringement charts until February 16, and you do not state that the supplemental charts will cure the other deficiencies we noted, e.g., the location of the serial debug pins in Claim 1. Unfortunately, this change of position on your part leaves us no alternative but to turn to the Court for its assistance in obtaining Motorola's contentions for the Vaglica '814 patent.

If you would like to discuss this matter further, please do not hesitate to contact me at your earliest convenience.

Yours truly,

James P. Bradley

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Re: *STMicroelectronics, Inc. v. Motorola,* Inc. Civil Action No. 4:03cv276

Dear Jim:

As I stated on our January 16th meet and confer, here is the further information on the description of Motorola embodying products: UDR means Uniform Design Rule, IDR means Integer Design Rule and NVM means non-volatile memory. The numerical designation before UDR and IDR means percentage of shrinkage, e.g. 80% UDR means 80% shrinkage of Uniform Design Rule.

We have also identified the vendors for hydrogen annealed wafers. Motorola's vendors are Komatsu and Shin-Etsu, but other vendors may produce such wafers; they were identified in Motorola's initial disclosures.

I ask again that STMicroelectronics NV (and by copy of this letter to Bruce Sostek that STMicroelectronics Inc.) produce information that permits Motorola to determine if ST NV, ST Inc or their affiliates manufacture or purchase hydrogen annealed wafers and what products of STNV, ST Inc. or their affiliates contain such wafers

Sincerely,

Hilda C. Galvan

cc: Bruce Sostek, Esq. (via facsimile)

EX 4

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091773-012016

January 28, 2004

VIA FACSIMILE

James P. Bradley, Esq.
Sidley, Austin, Brown & Wood, LLP
717 North Harwood Street, Suite 3400
Dallas, Texas 75201

Re: *STMicroelectronics, Inc. v. Motorola*, Inc. Civil Action No. 4:03cv276

Dear Jim:

On Friday, January 23rd, we discussed ST NV's contention that Motorola has failed to comply with Patent Rule 3-1 with respect to the Tobin and Vaglica patents. Despite our position that the infringement contentions submitted by Motorola on October 31, 2003, comply with Patent Rule 3-1, I agreed that Motorola would supplement its infringement claim charts for the Vaglica patent as follows: (1) infringement claim charts for each of the specific ST products that use the ARM7 processor; and (2) infringement claim charts for ST products that use the ARM9 processor. For Tobin, I agreed that Motorola would provide the following information regarding its embodying products: Motorola product number, wafer used in that Motorola product number, and vendor supplying the wafer.

I also agreed to let you know by Tuesday when Motorola would be providing the Vaglica infringement charts and the Tobin information. As you know, the Joint Claim Construction Statement is due on February 2, 2004. Because the parties have been working on that statement, it has been impossible to turn our attention to the infringement claim charts. However, we will do so next week and anticipate that we will have that information to you by February 16th, although we may have the Tobin information available prior to the February 16th.

If you would like to discuss this further, please do not hesitate to contact me.

Sincerely,

Hilda C. Galvan

cc: Bruce Sostek, Esq. (via facsimile)

DLI-5820953v1

EX 5

Exhibit B

Motorola's P.R. 3-1 Disclosure of Asserted Claims and Preliminary Infringement Contentions for U.S. Patent No. 5,084,814 to Vaglica et al.

(a) **Asserted Claims:** 1, 3, 8, 10, 13-14, 17, 20, 22-25 and 27-29.

(b) **Accused STMicro Products:** STM products containing ARM7 Family cores (*e.g.*, STw2400 containing the ARM7TDMI core, STM wireless and networking applications containing the ARM7TDMI core, STM SoC products containing the ARM7TDMI core), ARM9 Family cores (*e.g.*, STM's mobile internet ASSP line containing the ARM926EJ-S core, STM multimedia and other products containing the ARM PrimeXsys Wireless Platform, STM products containing the ARM9E Thumb Family core, STM Nomadik open multimedia platform containing the ARM9EJ core), and upon information and belief, ARM10 Family cores (*e.g.*, STM multimedia and other products containing the ARM1026EJ-S core) and ARM11 Family cores (*e.g.*, STM products containing the ARM1136JF-S core).

(c) **Claim Chart for Accused STMicro Products:** Attached below.

(d) STMicro infringes the asserted claims literally and/or by the Doctrine of Equivalents.

(e) **Priority Date:** October 30, 1987.

(f) Motorola Products: The following Motorola products incorporate each of the asserted claims of the '814 patent: MC68300, CPU32, QUICC, MC86HC16, MC68332, MC68HC12, MC68HC08, MPC500, MPC8540, MPC8560, i.MX21, SC56685VH7VR2, SC56685VH8VR2, SC56685VH9VR2, SC29305VF, SC29312VH, SC29312VG, SC29332VG, and SC29201VH.

INFRINGEMENT CLAIM CHART FOR VAGLICA, *ET AL.* - U.S. PATENT NO. 5,084,814

Claim	Claim Element	STMicro Product
	Claim 1	
1A	A data processor having first and second modes of operation for use in a data processing system comprising:	The ARM7 RISC processor embedded in STM products is a data processor having an ARM/THUMB state and DEBUG state modes of operation for use in a data processing system.[1] *See, e.g.*, Tab 3, Fig. 1-2, Chapter 8, 8.3.1; Tab 4, Fig. 1-2, Chapter 5, 5.3.1
1B	means for operating a parallel communication bus;	The ARM7 RISC processor includes means for operating a parallel communication bus to memory. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4.
1C	means for operating a serial communication bus, said serial communication bus is coupled to said data processor by means of a plurality of pins, each of said plurality of pins is either not used or is used only for development support functions while said data processor is in said first mode;	The ARM7 RISC processor includes serial debug pins that are used only for development support functions. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1; Chapter 8; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4; Chapter 5
1D	the data processor comprising:	*See* Claim 1A.
1E	means for sequentially executing, while in said first mode, a first plurality of instructions fetched from a memory by means of said parallel communication bus while in said first mode;	The ARM7 RISC processor includes means for executing instructions in ARM/THUMB state, fetched from a memory via the memory bus while in ARM/THUMB state. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1; Chapter 3, 3.1; Chapter 4; Chapter 10; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4; Chapter 2; Tables 1-2 - 1-7.
1F	means for sequentially executing, while in said second mode, a second plurality of instructions received by means of said serial communication bus while in said second mode, said means for executing a second plurality of instructions further comprising means for accessing said memory by means of said parallel communication bus while in said second mode; and	The ARM7 RISC processor in AD6522 includes means for executing instructions in DEBUG state and further includes means for accessing memory via the memory bus while in DEBUG state. *See, e.g.*, Tab 3, Chapter 8; Chapter 9; Tab 4, Chapter 5; Appendix B.
1G	mode switch means for switching between said first and second modes and for disabling said means for operating a serial communications bus while said data processor is in said first mode.	The ARM7 RISC processor includes switch means for switching between first and second mode and for operating a serial communication bus. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3; Chapter 9; Tab 4, Figs. 1-2, 1-3, 1-4; Chapter 5; Appendix B.

[1] Analyses for STM products containing ARM9 Family cores is similar. Upon information and belief, analyses for products containing ARM10 and ARM11 Family cores is similar. Motorola will attempt to obtain additional relevant information in discovery to confirm this contention.

Claim	Claim Element	STMicro Product
	Claim 3	
	The method of claim 1, further comprising:	*See* Claim 1.
3A	said mode switch means is responsive to an externally-provided signal to switch from said first mode of operation to said second mode of operation; and	The ARM7 RISC processor includes circuits that are responsive to an externally-provided signal to switch from ARM/THUMB state to DEBUG state. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3; 2-1 (DBGRQ); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGRQ).
3B	control means for disabling said mode switch means from switching to said second mode of operation.	The ARM7 RISC processor includes circuit elements responsive to an external signal for disabling the mode switch from ARM/THUMB state to DEBUG State. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3; 2-1 (DBGEN); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGEN).
	Claim 8	
8A	A data processor for executing each of a plurality of instructions, the data processor having a plurality of system resources and comprising:	The ARM7 RISC processor embedded in STM products is a data processor that executes each of a plurality of instructions and has a plurality of system resources, such as memory and serial communications bus. *See, e.g.*, Tab 3, 1-2; Figs. 1-1, 1-2, 1-3; Chapters 3, 4; Tab 4, 1-2; Figs. 1-2; 1-3; 1-4; Chapters 2, 3.
8B	first means for executing said instructions;	The ARM7 RISC processor includes a core for executing the instructions. *See, e.g.*, Tab 3, 1-2; Figs. 1-1, 1-2, 1-3; Chapter 3; Tab 4, 1-2; Figs. 1-2; 1-3; 1-4; Chapter 2.
8C	second means for utilizing the system resources in accordance with the execution by said first means of a first subset of said instructions;	The ARM7 RISC processor includes circuitry that utilizes system resources, such as memory, in accordance with the execution of the first subset of instructions. *See, e.g.*, Tab 3, 1-2; Figs. 1-1, 1-2, 1-3; Chapters 3, 4; Tab 4, 1-2; Figs. 1-2; 1-3; 1-4; chapters 2, 3.
8D	third means for providing access to at least one of the system resources in accordance with the execution by said first means of a second subset of said instructions;	The ARM7 RISC processor includes circuitry that provides access to the memory and the serial interface when debug instructions are executed. *See, e.g.*, Tab 3, Chapter 8; Chapter 9; Tab 4, Chapter 5; Appendix B.
8E	first communication means for providing instructions of said first subset to said first means, said first communication means is operative for communication in response to instructions of both said first and second subsets of instructions;	The ARM7 RISC processor includes parallel bus to memory for providing instructions to the circuitry that executes instructions in ARM/THUMB state. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3; Chapters 2, 3; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4.

Claim	Claim Element	STMicro Product
8F	second communication means distinct from said first communication means for providing instructions of said second subset to said first means, said second communication means is not operative for communication of instructions of said second subset in response to any instructions of said first subset of instructions; and	The ARM7 RISC processor includes serial ports for providing instructions only in DEBUG state. *See, e.g.*, Tab 3 Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1; Chapter 8; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; Chapter 5; Appendix B.
8G	fourth means coupled to said first means and to said second communication means for using said second communication means to indicate a status of said first means while said first means is executing instructions of said first subset.	The ARM7 RISC processor includes an output signal that indicates that the processor is in DEBUG state. This signal is coupled to the other signals and busses in the processor. *See, e.g.*, Tab 3 Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1 (DBGACK); Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGACK).
Claim 10		
	A data processing system according to claim 8 further comprising:	*See* claim 8.
10A	mode switch means for switching between said first and second subsets of said instructions, said mode switch means being responsive to an externally-provided signal to switch from said first subset to said second subset; and	The ARM7 RISC processor includes circuits that are responsive to an externally-provided signal to switch from ARM/THUMB state to DEBUG state. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3; 2-1 (DBGRQ); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGRQ).
10B	control means for disabling said mode switch means from switching to said second subset of said instructions.	The ARM7 RISC processor includes circuit elements responsive to an external signal for disabling the mode switch from ARM/THUMB state to Debug State. *See, e.g.*, Tab 3, Figs. 1-2, 1-2, 1-3; 2-1 (DBGEN); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGEN).
Claim 13		
13A	A data processor comprising:	The ARM7DMI RISC processor embedded in the STM products is a data processor. *See, e.g.*, Tabs 3-4.
13B	execution means for sequentially executing a plurality of instructions, said execution means having a first mode in which instructions of a first subset are executed and a second mode in which instructions of a second subset are executed;	The ARM7 RISC processor includes address register, address incrementer, register bank, multiplexer, barrel shifter, ALU and interconnecting buses. *See, e.g.*, Tab 3, Fig. 1-2. The ARM7 RISC processor includes a plurality of instructions that are provided in the ARM instruction set. *See, e.g.*, Tab 3, Table 4-1. The ARM7 RISC processor includes circuitry that places the ARM7 RISC processor in a first mode that provides normal program execution. *See, e.g.*, Tab 3, 8.1, third paragraph. The ARM7 RISC includes circuitry that places the ARM7 RISC processor in a second mode (*e.g.*, in a DEBUG state) in which a STM is inserted into the instruction pipeline. *See, e.g.*, Tab 3, 8.1.

Claim	Claim Element	STMicro Product
13C	communication means for providing said plurality of instructions to said execution means, said communication means operating in a master mode while providing instructions of said first subset and in a slave mode while providing instructions of said second subset, said communication means is coupled to a first plurality of pins and to a second plurality of pins, said communication means uses the first plurality of pins while providing instructions of the first subset and uses the second plurality of pins while providing instructions of the second subset, each of the second plurality of pins is either not used or is used only for development support functions while the communication means is providing instructions of the first subset;	The ARM7 RISC processor includes circuitry that include a TAP controller and bus splitter which provide instructions in normal program execution. *See, e.g.*, Tab 3, Figure 1-1. The ARM7 RISC processor includes circuitry that provides debug hardware extensions that allow user to stall the core from program execution, examine its internal state and the state of the memory system, and then resume program execution. *See, e.g.*, Tab 3, 8.2. The ARM7 RISC processor includes: A first plurality of pins D[31:0] and DIN[31:0] are used for bidirectional data transfers between processor and external memory and for transfer of instructions and data between processor and memory. *See, e.g.*, Tab 3, Fig. 1.1. A second plurality of pins TDI and TDO, respectively, provide test data input, output from the boundary scan logic. *See, e.g.*, Tab 3, Fig. 1.1.
13D	mode switch means for switching between said first mode and said second mode and for preventing said communication means from operating in said slave mode while said execution means is executing instructions of said first subset.	The ARM7TDMI RISC processor is forced into debug state after a breakpoint, watchpoint or debug-request has occurred. *See, e.g.*, Tab 3, 8.3. The ARM7 RISC processor includes circuits that are responsive to an externally-provided signal to switch from ARM/THUMB state to DEBUG state. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3; 2-1 (DBGRQ); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGRQ).
Claim 14		
	A data processor according to claim 13 wherein said communication means further comprises:	*See* claim 13.
14A	controller means for operating a parallel communication bus as a bus master; and	The ARM7TDMI RISC processor includes circuitry for operating the parallel communications bus to memory as a bus master. *See, e.g.*, Tab 3, 1-2; Figs. 1-1, 1-2, 1-3; 2-1; Chapter 6; Tab 4, Figs. 1-2; 1-3, 1-4; Chapter 3.
14B	a slave-only serial communication interface.	The ARM7TDMI RISC processor includes circuitry for operating the serial communications interface. *See, e.g.*, Tab 3, 1-2; Figs. 1-1, 1-2, 1-3; 2-1; Chapter 8; Tab 4, Figs. 1-2, 1-3, 1-4; Chapter 5.
Claim 17		
	A data processor according to claim 13 wherein:	*See* claim 13.

Claim	Claim Element	STMicro Product
17	said mode switch means is responsive to an externally-provided signal to switch from said first mode to said second mode.	The ARM7TDMI RISC processor is forced into debug state after a breakpoint, watchpoint or debug-request has occurred. *See, e.g.*, Tab 3, 8.3. The ARM7 RISC processor includes circuits that are responsive to an externally-provided signal to switch from ARM/THUMB state to DEBUG state. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3; 2-1 (DBGRQ); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGRQ).
	Claim 20	
	A data processor according to claim 13 further comprising:	*See* claim 13.
20	control means for disabling said mode switch means from switching to said second mode of operation.	The ARM7 RISC processor includes circuit elements responsive to an external signal for disabling the mode switch from ARM/THUMB state to Debug State. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3, 2-1 (DBGEN); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGEN).
	Claim 22	
22A	An integrated circuit data processor comprising: execution means for sequentially executing a plurality of instructions	The ARM7TDMI RISC processor embedded in the STM products is a data processor containing means for sequentially executing a plurality of instructions. *See, e.g.*, Tabs 3 and 4.
22B	first communication means for operating a first communication bus as a bus master to provide a first subset of said plurality of instructions to said execution means;	The ARM7 RISC processor includes means for operating a parallel communication bus to memory. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4.
22C	second communication means for operating a second communication bus as a bus slave to provide a second subset of said plurality of instructions to said execution means; and	The ARM7 RISC processor includes serial debug pins that are used only for development support functions and provide debug instructions. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3, 2.1; Chapter 8; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4; Chapter 5.
22D	mode switch means for switching said execution means between said first and second subsets of said plurality of instructions and for enabling said second communication means only while said execution means is executing instructions of said second subset;	The ARM7TDMI RISC processor is forced into debug state after a breakpoint, watchpoint or debug-request has occurred. *See, e.g.*, Tab 3, 8.3. The ARM7 RISC processor includes circuits that are responsive to an externally-provided signal to switch from ARM/THUMB state to DEBUG state. *See, e.g.*, Tab 3, Figs. 1-1, 1-2, 1-3; 2-1 ((DBGRQ); Tab 4, Figs. 1-2, 1-3, 1-4; 5.3.1 (DBGRQ). Debug state instructions are only enabled while the processor is in DEBUG state. *See, e.g.*, Tab 3, Chapter 8; Tab 4, Chapter 5; Appendix B, B.5, B.6. The serial communications port is enabled during DEBUG state. *See, e.g.*, Tab 3, Chapter 8; Tab 4, Chapter 5; Appendix B.

Claim	Claim Element	STMicro Product
22E	wherein said second communication bus is coupled to said data processor by means of a plurality of pins, said plurality of pins are either not used or are used only for development support functions while said data processor is executing instructions of said second subset.	A first plurality of pins D[31:0] and DIN[31:0] are used for bidirectional data transfers between processor and external memory and for transfer of instructions and data between processor and memory. *See, e.g.*, 3, Fig. 1-1, 2-1, pp. 2-4, 2-5; Tab 4, Figs. 1-2, 1-3, 1-4; 2-1. A second plurality of pins TDI and TDO, respectively, provide test data input, output from the boundary scan logic. *See, e.g.*, Tab 3, Figure 1.1; p. 2-10; Tab 4, Figs. 1-2, 1-3, 1-4; 2-1.
Claim 23		
	An integrated circuit data processor according to claim 22 wherein:	*See* claim 22.
23	said first communication means is operative in response to the execution by said execution means of instructions of both said first and second subsets.	The parallel interface to memory in the ARM7TDMI RISC processor is operative in both ARM/THUMB state and in DEBUG state. *See, e.g.*, Tab 3, Chapters 1, 8, 9; Tab 4, Chapter 5, Appendix B.
Claim 24		
	An integrated circuit data processor according to claim 22 further comprising a plurality of pins for interconnection of the data processor with external devices and wherein:	*See* claim 22.
24A	said first communication means utilizes a first subset of said plurality of pins;	A first plurality of pins D[31:0] and DIN[31:0] are used for bidirectional data transfers between processor and external memory and for transfer of instructions and data between processor and memory. *See, e.g.*, Tab 3, Fig. 1-1, Fig. 2-1, pp. 2-4, 2-5; Tab 4, Figs. 1-2, 1-3; 1-4; 2-1.
24B	said second communication means utilizes a second subset of said plurality of pins, said second subset of said plurality of pins being inaccessible to said execution means for providing said second subset of said plurality of instructions to said execution means while executing instructions of said first subset.	A second plurality of pins TDI and TDO, respectively, provide test data input, output from the boundary scan logic. *See, e.g.*, Tab 3, Fig. 1-1, 2-1, p. 2-10; Tab 4, Figs. 1-2, 1-3, 1-4; 2-1.
Claim 25		
	An integrated circuit data processor according to claim 24 wherein:	*See* claim 24.
25A	said execution means further comprises an instruction pipe; and	The ARM7 RISC processor includes an instruction pipeline. *See, e.g.*, Tab 3, Fig. 1-2; Tab 4, Fig. 1-3.
25B	at least one of said second subset of said plurality of pins is used while said execution means is executing instructions of said first subset to provide an output indicating an activity of said instruction pipe.	The ARM7 RISC processor includes signals that provide an output indicating an activity of the instruction pipe. *See, e.g.*, Tab 3, 4.3, 8.14, Table 8-4 (Scan Chain 1, bit no. 56).

Claim	Claim Element	STMicro Product
	Claim 27	
27A	An integrated circuit data processor comprising:	The ARM7TDMI RISC processor embedded in the STM products is a data processor. *See, e.g.*, Tabs 3 and 4.
27B	a central processing unit, the central processing unit further comprising:	The ARM7 RISC processor includes a central processing unit. *See, e.g.*, Tab 3, Chapter 1, 1.1, Figs. 1-1, 1-2, 1-3; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4.
27C	program counter means for storing an address;	The ARM7 RISC processor includes a program counter for storing an address. *See, e.g.*, Tab 3 3.7.1 (Register 15/Program Counter); Tab 4, 2.6.1 (Register 15/Program Counter).
27D	execution means for executing a first plurality of instructions while in a first operating mode, for executing a second plurality of instructions while in a second operating mode, for producing instruction prefetch requests, for determining a sequence of instruction execution and for storing addresses in the program counter means in accordance with the sequence; and	The ARM7 RISC processor includes means for executing instructions in ARM/THUMB state, fetched from a memory via the memory bus while in ARM/THUMB state. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1; Chapter 3, 3.1; Chapter 4; Chapter 10; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4, 1.4; Chapter 2; Tables 1-2 - 1-7. The ARM7 RISC processor includes means for executing instructions in DEBUG state, and includes means for accessing memory via the memory bus while in DEBUG state. *See, e.g.*, Tab 3, Chapter 8, Chapter 9; Tab 4, Chapter 5; Appendix B. The ARM7 RISC processor includes circuitry for producing instruction prefetch requests, for determining a sequence of instruction execution and for storing addresses in the program counter means. *See, e.g.*, Tab 3, Fig. 1-1, 1-2; 4.4; Tab 4, 6.1.
27E	bus controller means for coupling the central processing unit to a parallel communication bus and for operating the parallel communication bus as a bus master, in response to one of the instruction prefetch requests from the execution means, to obtain one of said first plurality of instructions from a location in a memory specified by the address stored in the program counter means; and	The ARM7 RISC processor includes means for operating a parallel communication bus to memory as a bus master in response to one of the instruction prefetch requests from the execution means, to obtain one of said first plurality of instructions from a location in a memory specified by the address stored in the program counter means. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3; 2.1; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4.
27F	a plurality of resources under control of the central processing unit for performing a predetermined plurality of functions while in the first operating mode, the predetermined plurality of functions comprises substantially all of the functions which the data processor is capable of performing;	The ARM7 RISC processor has a plurality of system resources, such as memory and serial communications bus under its control and substantially all of the instruction set of the ARM7 RISC processor are available in ARM/THUMB state. *See, e.g.*, Tab 3, 1-2; Figs. 1-1, 1-2, 1-3; Chapters 3, 4; Tab 4, 1-2; Figs. 1-2; 1-3; 1-4; Chapters 2, 3.
27G	wherein the improvement comprises:	

Claim	Claim Element	STMicro Product
27H	a serial communication bus means coupled to the execution means for providing one of said second plurality of instructions to the execution means under control of an external serial bus master, the serial communication bus is not operative for serial communication while in the first operating mode;	The ARM7 RISC processor embedded in AD6522 includes serial debug pins that are used only for development support functions. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3, 2.1; Chapter 8; Tab 4, Chapter 1, Figs. 1-2, 1-3; 1-4; 1.4; Chapter 5.
27I	the execution means ceases to produce the instruction prefetch requests while in the second operating mode, ceases to determine the sequence of instruction execution while in the second operating mode and ceases to store addresses in the program counter means in accordance with the sequence while in the second operating mode; and	The ARM7 RISC processor includes signals that can be used to halt the execution means. *See, e.g.*, Tab 3, 2.1 (BREAKPT); Chapters 8, 9; Tab 4, Chapter 5; Appendix B.
27J	the plurality of resources performs each of said predetermined plurality of functions while in the second operating mode.	The ARM7 RISC processor embedded in AD6522 includes means for executing instructions in DEBUG state and further includes means for accessing memory via the memory bus while in DEBUG state. *See, e.g.*, Tab 3, Chapter 8; Chapter 9; Tab 4, Chapter 5; Appendix B.
Claim 28		
	An integrated circuit data processor according to claim 27 wherein:	*See* claim 27.
28	the serial communication bus means is operative while in the first mode of operation to provide an output indicating a current activity of the central processing unit.	The ARM7 RISC processor embedded in AD6522 includes serial debug pins that are used only for development support functions including examining scan chains that indicate the current activity of the central processing unit. *See, e.g.*, Tab 3, Chapter 1, Figs. 1-1, 1-2, 1-3, 2.1; Chapter 8; Tab 4, Chapter 1, Figs. 1-2, 1-3, 1-4; 1.4; Chapter 5; Appendix B.
Claim 29		
	An integrated circuit data processor according to claim 27 wherein:	*See* claim 27.
29A	the central processing unit further comprises:	*See* claim 27.
29B	instruction pipe means under control of the execution means for storing instructions obtained by the bus controller means while in the first mode of operation and instructions provided by the serial communication bus means while in the second mode of operation; and	The ARM7 RISC processor includes an instruction pipeline for storing instructions obtained by the bus controller while in the first mode of operation and instructions provided by the serial communications bus while in the second mode of operation. *See, e.g.*, Tab 3, Fig. 1-2; Tab 4, Fig. 1-3.
29C	the serial communication bus means is operative in [*sic*] while in the first mode of operation to provide an output indicating an activity of the instruction pipe means.	The ARM7 RISC processor includes signals that provide an output indicating an activity of the instruction pipe. *See, e.g.*, Tab 4, 4.3, 8.14, table 8-4 (Scan Chain 1, bit no. 56).

Exhibit C

Motorola's P.R. 3-1 Disclosure of Asserted Claims and Preliminary Infringement Contentions for U.S. Patent No. 4,548,654 to Tobin.

(a) **Asserted Claims:** 1-7, 9.

(b) **Accused STMicro Products:** Processes used by or for STM which include the step of heating a silicon wafer or substrate in a reducing ambient and a later step of heating the wafer or substrate at a lower temperature, and the STM products made thereby. Motorola currently does not have access to STM's process flow information or the process flow information from STM's wafer suppliers. Motorola's inaccessibility to this information hinders its limitation-by-limitation preliminary infringement analysis.

Upon information and belief, STM obtains silicon wafers from at least four sources. While the proprietary processes that these wafer suppliers use to produce denuded wafers is not publicly available, published literature and confidential information available to Motorola suggests that these suppliers prepare or fabricate silicon wafers or substrates using the process steps identified above. *See, e.g., Collection of Publicly Available Articles at Tab 5.*[1]

(c) **Claim Chart for Accused STMicro Products:** Attached below.

(d) STMicro infringes the asserted claims literally and/or by the Doctrine of Equivalents.

(e) **Priority Date:** June 3, 1983.

[1] Motorola has additional materials from these suppliers which it cannot produce at this time because the suppliers may consider these materials to be confidential. Motorola is attempting to get permission from the suppliers to produce these materials to STM, and Motorola will do so promptly upon receiving such permission.

(f) Motorola Products: Upon information and belief, the following Motorola products are made by processes that incorporate each of the asserted claims of the '654 patent:[2] 80% UDR, 82.5% UDR, 50% IDR, 60% IDR, 73% IDR, NVM (all 150 mm wafers), SGF (split gate flash, HiP6W RF).

[2] Motorola obtains the applicable silicon wafers from various sources. Because these sources consider the relevant process information to be confidential, Motorola is attempting to obtain this information to confirm this contention.

INFRINGEMENT CLAIM CHART FOR TOBIN - U.S. PATENT NO. 4,548,654

Claim	Claim Element	STMicro Process / Product
	Claim 1	
1A	A process for preparing a silicon substrate for the fabrication of a device which comprises the steps of:	The accused processes prepare silicon substrates for the fabrication of semiconductor devices. The resultant devices are accused products.
1B	providing a silicon substrate having a concentration of oxygen incorporated therein;	A silicon substrate having an oxygen concentration is provided.
1C	heating said substrate to a first elevated temperature in a reducing ambient;	The substrate is heated to a first temperature in a reducing ambient.
1D	lowering the temperature of said substrate to a second elevated temperature lower than said first elevated temperature; and	The temperature of the substrate is lowered to a second elevated temperature.
1E	maintaining said substrate at said second elevated temperature for a time to allow nucleation of oxygen precipitates in the bulk of said substrate.	The lower temperature is maintained to allow nucleation of oxygen precipitates in the bulk of the substrate.
	Claim 2	
2	The process of claim 1 wherein said reducing ambient comprises hydrogen.	See Claim 1. Additionally, the reducing ambient includes hydrogen.
	Claim 3	
3	The process of claim 2 wherein said reducing ambient comprises hydrogen diluted with argon or helium.	See Claim 1. Additionally, the reducing ambient includes hydrogen diluted with argon or helium.
	Claim 4	
4	The process of claim 1 wherein said concentration of oxygen exceed 1.3×10^{18} cm^{-3}.	See Claim 1. Additionally, the oxygen concentration exceeds 1.3×10^{18} cm^{-3}.
	Claim 5	
5	The process of claim 1 wherein said first temperature comprises a temperature between about 1000° and 1200° C.	See Claim 1. Additionally, the substrate is heated to a first temperature between about 1000° and 1200° C.
	Claim 6	
6	The process of claim 1 wherein said second elevated temperature is about 600° - 800° C.	See Claim 1. Additionally, the substrate is heated to a said second elevated temperature between about 600° - 800° C.
	Claim 7	
7	The process of claim 5 wherein said first temperature is about 1100°-1150° C.	See Claim 1. Additionally, the first temperature is between about 1100° C - 1150° C.

Claim	Claim Element	STMicro Process / Product
	Claim 9	
9A	A process for fabricating a semiconductor device which comprises the steps of:	The accused processes prepare silicon semiconductor devices. The resultant devices are accused products.
9B	providing a silicon wafer of first conductivity type having a concentration of oxygen incorporated therein;	A silicon wafer of a first conductivity type having an oxygen concentration is provided.
9C	heating said wafer to a temperature between about 1000° and 1200° C. in a reducing ambient for a sufficient time to form a denuded surface layer on said wafer; heating said wafer in an oxidizing ambient to form a protective oxide on the surface thereof; reducing the temperature of said wafer to a second temperature between about 600° and 800° C. to nucleate the precipitation of oxygen in the bulk of said wafer; and	The wafer heated to a first temperature between about 1000° and 1200° C. in a reducing ambient to form a denuded surface layer on the wafer. The wafer is heated in an oxidizing ambient to form a protective oxide on the wafer's surface. The temperature is reduced to between about 600° and 800° C. to nucleate the precipitation of oxygen in the bulk of the wafer.
9D	forming regions of second conductivity type in said denuded surface layer, said regions having a depth into said wafer less than the thickness of said surface layer.	Regions of a second conductivity type are formed in the denuded surface layer. The depth of these regions into the wafer is less that the thickness of the denuded surface layer.

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January 30, 2004

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VIA FACSIMILE (214) 969-5100

Re: *STMicroelectronics, Inc. v. Motorola, Inc. v. STMicroelectronics N.V. and STMicroelectronics, Inc.* Civil Action No. 4:03-CV-276 (Sherman)

Dear Hilda:

I called you last Friday, January 23, 2004, in an another effort to have Motorola comply with Patent Rule 3-1. When I did not receive supplemental infringement contentions for Tobin on Tuesday, the date I understood you would provide these, I decided to send you an e-mail that set forth our understanding of your offer to supplement Motorola's infringement contentions and claim charts for the Tobin and Vaglica patents. We were surprised to receive your letter Wednesday evening with your different understanding of what Motorola agreed to do. Leaving the differences aside on our understanding from the call, we continue to seek Motorola's infringement contentions that are required by P.R. 3-1.

The Tobin '654 Patent

With respect to the Tobin '654 patent, you stated on our call that you were unable to identify at this time any ST Inc. or ST NV process that infringes the '654 patent. You were also unable to identify any wafer purchased by ST Inc. or ST NV that was used in fabricating a semiconductor device that you contend infringes the '654 patent. We understood you to say that you agreed to identify the wafers purchased by ST Inc. or ST NV that you contend infringe the Tobin '654 patent by last Tuesday. The offer you make in Wednesday's letter for Motorola to provide information regarding wafers used in Motorola products that practice the claimed invention is entirely different and not in compliance with the rules. P.R. 3-1(f) gives a patentee the option of identifying its own products that practice its patents, but this does not put Motorola in compliance with P.R. 3-1(c).

In view of the fact that Motorola has failed to identify any product or process that infringes the '654 patent, it is clear that Motorola has failed to comply with P.R. 3-1(b) or P.R. 3-1(c). We feel we have now exhausted our efforts to have Motorola fulfill its obligations under P.R. 3-1, and, thus, you leave us with no choice but to seek the Court's assistance in this matter.

The Vaglica '814 Patent

On January 23, we also met and conferred regarding Motorola's deficiencies in its infringement contentions for the '814 patent. In addition to failing to include any ST Inc. or ST NV products in the charts, the charts were deficient in failing to identify where each element was found in the ARM 7 cores. We understood you agreed to provide infringement claim charts for the Vaglica '814 patent as you apply it to ST Inc. or ST NV products by Friday, January 30, 2004. You now inform us that you will not provide these infringement charts until February 16, and you do not state that the supplemental charts will cure the other deficiencies we noted, e.g., the location of the serial debug pins in Claim 1. Unfortunately, this change of position on your part leaves us no alternative but to turn to the Court for its assistance in obtaining Motorola's contentions for the Vaglica '814 patent.

If you would like to discuss this matter further, please do not hesitate to contact me at your earliest convenience.

Yours truly,

James P. Bradley

JPB/bls

cc: Mike Jones, Esq. (via facsimile)
Bruce S. Sostek, Esq. (via facsimile)
Jane P. Brandt, Esq. (via facsimile)
Kevin P. Ferguson, Esq. (via facsimile)

bcc: Kevin Fillip, Esq. (via facsimile)
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